Identifying Phase Noise Sources in a PLL

Design File: DN002 15 October 1999

Introduction

Many modern communication systems utilise PLL frequency synthesizers, commonly with specifications on phase noise performance. This report details a simple technique that we have found valuable in isolating the sources of phase noise in a PLL synthesizer, and is especially useful when only a spectrum analyser is available for measurements. An additional passive filter (which we nicknamed a "PLL Widget") is added to the PLL, greatly narrowing the loop bandwidth, causing the output phase noise to approximate that from the VCO alone. Inspection of the output phase noise in the normal and reduced bandwidth modes enables the source of the phase noise to be tracked down to either the VCO or PLL.

The PLL widget is a small passive device and may be plugged in place of link on the VCO control line, enabling the bandwidth to be easily reduced during development. The device can also be used in measuring the frequency domain characteristics of the PLL, including loop gain and phase margin. This is the subject of a separate report [1].

Sources of Phase Noise

The output phase noise of any PLL synthesizer comes from many sources including:

1. VCO phase noise
    a. Basic VCO phase noise
    b. VCO excess phase
2. Divider and phase detector noise
3. Noise from the resistors and active devices in the loop filter

The Basic VCO phase noise is that measured for an isolated VCO operating with noise free power supply and noise free control line. VCO excess phase noise is caused by interference in its current environment, due primarily to power supply noise but may include other interference from the nearby PLL components. Sources 2 and 3 contribute to the output phase noise by modulating the VCO control line.

Identifying Phase Noise Sources

In order to improve the output phase noise, it is necessary to identify the sources. In well equipped laboratories, it may be possible to measure the phase noise of the VCO in isolation, and then in the PLL. The added noise from the PLL can then be clearly identified. Such a measurement is shown in the following figure:

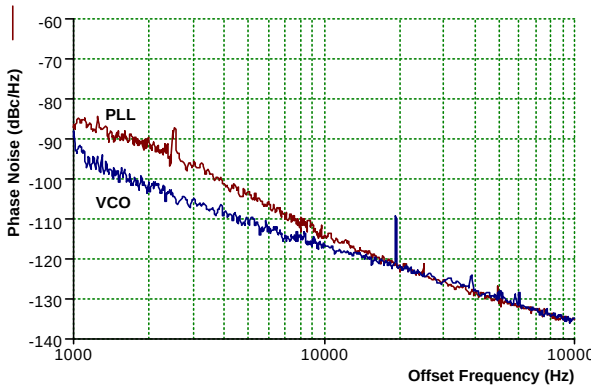

Figure 1 - Phase Noise of Isolated VCO (VCO) and of VCO Locked in PLL (PLL)

In Figure 1 it can be seen that in this synthesizer the VCO dominates the phase noise above 20kHz and the PLL below this. If it were necessary here to reduce the phase noise at 10kHz, then it would be the PLL that needs most modification, not the VCO.

Assuming that some form of spectrum analyser is available for measuring the phase noise, the locked VCO is easily measured, what is more difficult is measuring the VCO without the PLL. This can be done with batteries supplying the control voltage, however stability is a major problem and the measurement is very fiddley. We will show how the PLL may be modified to reduce the PLL bandwidth and to significantly attenuate the contribution of PLL noise sources to the output phase noise. This often approximates measuring the VCO in isolation.

The PLL

A typical PLL synthesiser is shown in Figure 2. Although not essential, it is convenient when prototyping to include a link on the VCO control line. This allows the loop to be broken for VCO testing, as well as allowing the insertion of additional filtering.

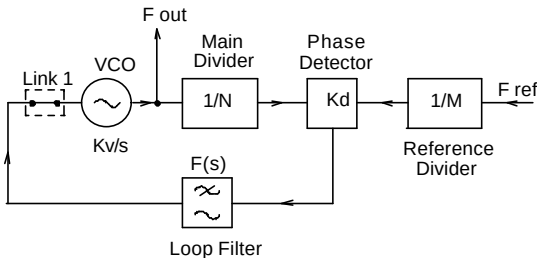

Figure 2 - PLL Synthesizer

Designing the "Widget"

The design will be demonstrated by means of an example. Assume that the PLL under investigation has a loop bandwidth of 10kHz, with compensating zero at 330Hz and additional pole at 3kHz.

We will design a "PLL widget" that can be inserted in place of "Link 1" in Figure 1, that will reduce the PLL bandwidth from 10kHz to 1kHz. The original PLL loop gain is indicated in Figure 3.

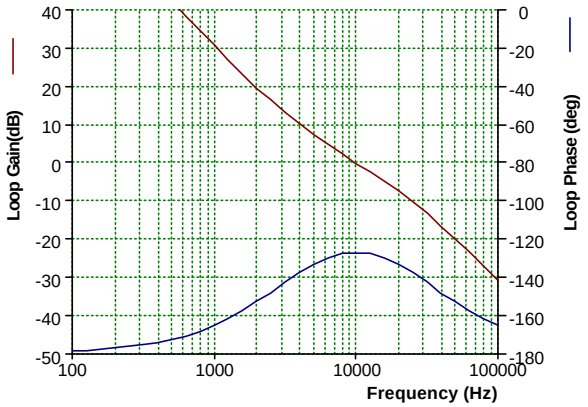

Figure 3 - PLL Loop Response

With a bandwidth of 10kHz and a compensating zero at 330Hz, the loop gain at 1kHz is approximately 30dB. Thus to reduce the loop bandwidth to 1kHz, the Widget must have 30dB of attenuation at 1kHz. Additionally, the device must improve on the phase margin at 1kHz which is around 15° in Figure 3. Other requirements on the widget are:

- no attenuation at DC (this would reduce the voltage swing available to drive the VCO)
- significant attenuation (say ≥ 20dB) at frequencies above 1kHz.

A simple circuit that meets the requirement of no attenuation at DC and significant attenuation above that is shown in Figure 4:

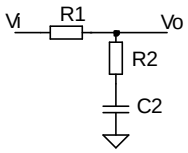

Figure 4 - Circuit 1

The transfer function of circuit 1 is

$$\frac{V_o}{V_i} = \frac{1 + sR_2C_2}{1 + s(R_1 + R_2)C_2}.$$

Note that we are assuming that the output impedance of the loop filter is very low (e.g. op-amp output) and that the input impedance of the VCO is high. The low output impedance is only really correct for active loop filters, if passive filters are used then the widget design is complicated by the need to use a low-noise buffer amplifier. We will not consider this case here.

Choosing some convenient values (not particularly critical) $R_1 = 100\text{k}$, $R_2 = 1\text{k}$ and $C_2 = 10\mu\text{F}$ gives a pole at 0.16Hz and a zero at 16Hz. The response is shown in Figure 5:

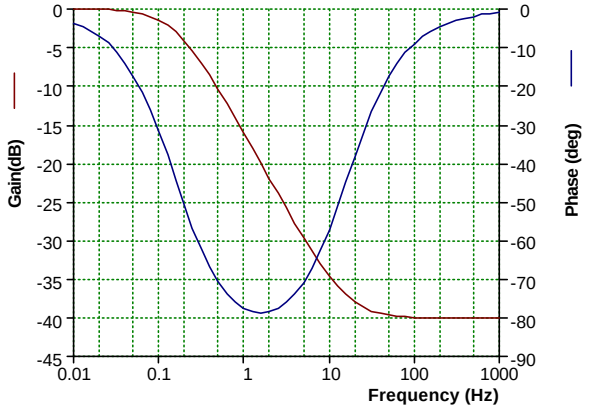

Figure 5 – Response of Circuit of Fig 4

This provides 40dB of attenuation for frequencies above 100Hz, however it provides no phase lead, so if inserted in the PLL the loop will be unstable. To provide phase lead at 1kHz, we introduce a zero at 300Hz and a pole at 3kHz (to prevent the gain returning to unity at high frequencies). The result is a network as follows:

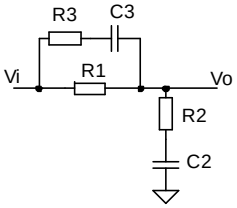

Figure 6 – Circuit of Widget

The zero locations and approximate pole locations for this circuit are as follows:

Zeroes:

$$f_{z1} = \frac{1}{2\pi R_2 C_2}$$

$$f_{z2} = \frac{1}{2\pi (R_1 + R_3)C_3}$$

Poles: (assuming $R_3C_3 << R_2C_2$ and $C_3 << C_2$)

$$f_{p1} = \frac{1}{2\pi (R_1 + R_2)C_2}$$

$$f_{p2} = \frac{1}{2p\,(R_3 + \frac{R_1 R_2}{R_1 + R_2})C_3}$$

$$\approx \frac{1}{2p\,(R_3 + R_2)C_3} \quad \text{for} R_1 >> R_2$$

For our example, adding a zero at 300Hz and a pole at 3kHz gives R1 = 100k, R2 = 1k, C2 = 10µF, R3 = 10k and C3 = 4.8nF, with the response as follows:

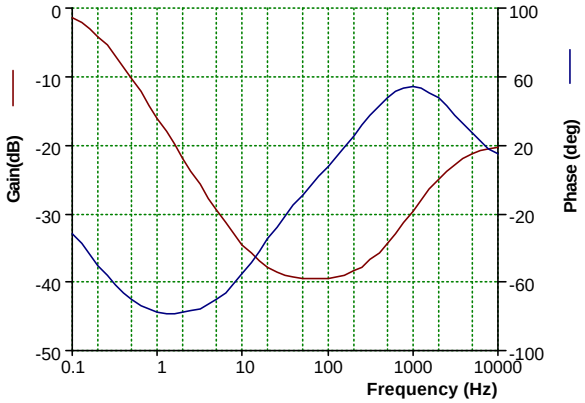

Figure 7 - Transfer Function of Widget

Note the ≥20dB of attenuation above 2Hz and around 50° of phase lead at 1kHz. The loop gain for the PLL with the widget in place is shown below:

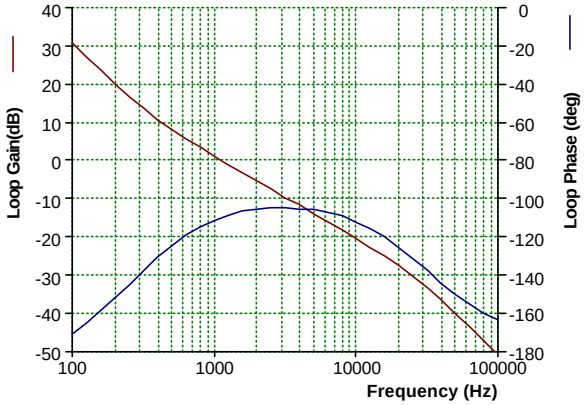

Figure 8 - Modified PLL Loop Gain

The PLL will now lock with a loop bandwidth of 1kHz. Sources of phase noise from the PLL are attenuated by over 20dB and thus, by inspecting the new output spectrum, the contribution to output phase noise from VCO modulation may be deduced.

If the link in the PLL is made using standard 0.1inch links, and if a ground pin is made available, then the PLL widget may be made on a small header and simply plugged in when needed.

Note that it is important to consider the effect of the widget on the phase noise. It is necessary to choose the impedance level of the widget so that the phase noise is not degraded significantly. For this example, the major contribution to the output phase noise above 1kHz is the noise from R2, i.e 4nV/√Hz. The significance of this depends on the VCO K_v and the phase noise specifications. The phase noise at offset frequency f_m caused by resistor R_2 is given by

$$L_f(f_m) = 20\log\left(\frac{K_v\sqrt{2kTR_2}}{f_m}\right)\text{dBc/Hz}$$

where $k = 1.38\times10^{-23}$ and $T = 300K$

Note that it is often difficult to make a suitable widget in very low phase noise applications.

An example of a measurement using a widget is shown in the following figure:

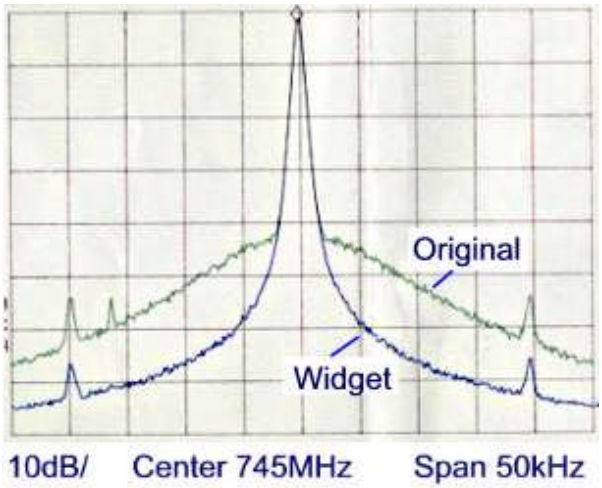

Figure 9 - Measured Spectrum of PLL Synthesiser

For the synthesizer shown in Figure 9 it can be clearly seen that the phase noise is dominated by the PLL components. The PLL spectrum could be improved to that shown with the Widget by using lower noise loop components (phase detector, loop filter) or lowering the loop bandwidth (which is what was in fact done using the widget).

Conclusion

A "PLL Widget" has been described that can be easily plugged into a PLL, dramatically narrowing the loop bandwidth. This allows the easy measurement of a spectrum approximating that of the VCO alone, facilitating the determination as to whether the PLL or VCO is limiting the phase noise performance.

REFERENCES:

1. "Measuring PLL Loop Bandwidth" DN003 Applied Radio Labs 1999

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