Measuring the Loop Bandwidth of a PLL

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Introduction

Many modern communication systems utilise PLL frequency synthesizers. The PLL is a feedback loop, and the frequency domain characteristics of the loop transfer function (gain and phase response) have significant effect on the PLL operation, for example:

- Locking times (e.g. overshoot and ringing for poor phase margin)
- Phase noise 'ears' if phase margin is poor
- Frequency response of modulation / demodulation

Despite the significance of the PLL loop gain on loop performance, there seem to be few well-known measurement techniques.

This report describes simple techniques for measuring the PLL open loop transfer function (amplitude and phase).

We initially developed techniques for measuring the loop bandwidth directly when we were investigating synthesizer locking problems. We have since found it a valuable design verification and diagnostic tool in many applications including:

- Investigating locking difficulties (measuring phase margin)
- Confirming that phase noise improvements from PLL modifications are not due to loop bandwidth reduction
- Determining loop gain for modulation loops

Note that the loop gain and phase is accurately measured, including effects that are sometimes omitted from design analysis, for example:

- Phase shift caused by the delay of digital or sampling phase detectors
- Additional poles due to decoupling (e.g. an RC decoupling circuit is often added at the VCO input)

The PLL

A typical PLL synthesiser is shown in Figure 1. We assume that a link has been included on the VCO control line. This allows the loop to be broken for VCO testing, as well as allowing the insertion of additional filtering during testing.

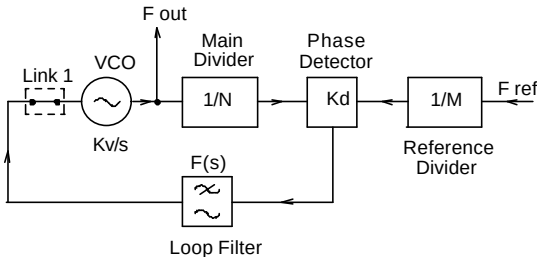

Figure 1 - PLL Synthesizer

Measuring the Loop Bandwidth

For the PLL in Figure 1, we insert a low-pass filter in place of Link 1. A suitable filter is the "PLL Widget" described in [1]. We assume that the loop filter has a low output impedance. In this case, we consider the effect of coupling a test signal in to the VCO control line as shown in Figure 2.

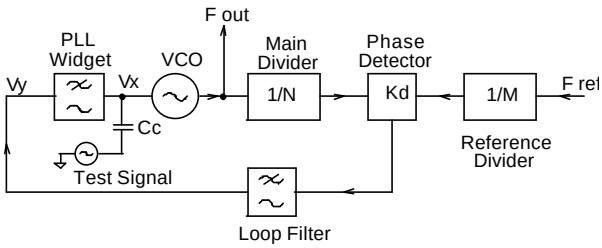

Figure 2

Denoting the original PLL loop gain by $G(s)$, then

$$V_y = G(s)V_x \qquad \ldots (1)$$

This is true if the output impedance of the loop filter is low so that V_y is independent of the load on the filter, and in particular, has no component caused by V_x leaking back through the PLL Widget.

Equation (1) shows that as long as we can inject some suitable signal into the PLL, we can measure the loop gain $G(s)$ by measuring V_y and V_x.

Note that the object inserted in place of the link need not be as complicated as the PLL widget, but if a suitable widget is available it may be used. A simple resistor may be used as long as it is much larger than the output impedance of the loop filter, and the extra pole caused by the resistor and the coupling capacitor

(and any input capacitance of the VCO) does not cause stability problems.

If the loop filter does not have a low output impedance then it is possible to modify the widget to include a buffer amplifier at the input, in order to provide the needed isolation.

The simplest arrangement we use to measure the loop bandwidth and phase margin needs only a function generator and a dual-trace oscilloscope. The arrangement is shown in Figure 3

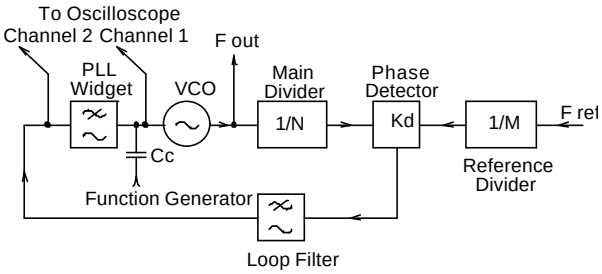

Figure 3

The function generator level is set to provide adequate signal on the oscilloscope, whilst not sending the PLL out of lock. In setting this it is wise to monitor the phase detector output to check that large phase excursions are not occurring (i.e. that the loop is staying linear).

When suitable levels have been found, it is a simple matter to alter the frequency of the function generator to find the frequency where the two amplitudes are equal. This is the unity gain frequency. The phase margin can be determined by measuring the phase shift between the signals, either by determining the time delay between the signals dual trace mode, or by using the XY display on the oscilloscope.

If a suitable piece of equipment is available that can measure audio transfer functions, then the amplitude and phase of the loop gain can be measured. We use a HP4195A Network / Spectrum Analyser. In this case the network analyser source is connected in place of the function generator, and the network analyser is configured to measure $\frac{V_y}{V_x}$. Again, it is important to set the level so as the phase excursions at the phase detector are modest. An example of the loop gain measured for a PLL with a 5kHz bandwidth is shown in Figure 4.

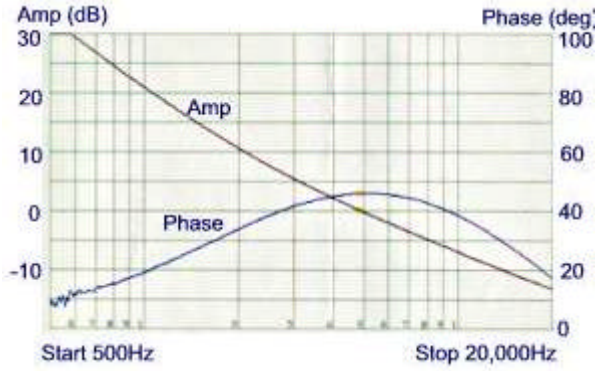

Figure 4 - Loop Gain and Phase Measurement

The measured phase margin is about 46° at 5kHz.

Conclusion

The loop bandwidth and phase margin of a PLL synthesizer may be measured using the techniques given. This a useful for PLL diagnostics as well as design verification.

REFERENCES:

1. "Identifying Phase Noise Sources in a PLL" DN002, Applied Radio Labs 1999

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