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Understanding Phase Noise From Digital Components in PLL Frequency Synthesizers

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Introduction

The phase noise of a Phase Locked Loop (PLL) frequency synthesizer can be a key parameter in a communications system design. Being able to model the phase noise and to predict it with some accuracy is a desirable engineering goal.

The sources of phase noise within a PLL synthesizer include:

1. VCO phase noise
2. Reference oscillator phase noise
3. Thermal noise and device noise from components in the loop filter
4. Noise from the digital dividers and phase detector

Noise sources 1 – 3 are well understood and can usually be modelled with good accuracy using measured phase noise data for the VCO and reference, and conventional noise models from circuit theory for the loop filter. The one area that is not well understood is the noise contributions from the digital devices; the dividers and digital phase detector. The dividers and phase detector are often integrated in one monolithic integrated circuit, so it is common to speak of the noise from the digital components as the noise from the PLL IC.

A notable contribution to understanding the noise from the digital components is a recent publication by Banerjee [1] which proposes a simple empirical model which is shown to give useful accuracy. This model has been successful implemented in a comprehensive PLL synthesizer analysis program [2]. This paper builds on the explanations given in [1] and derives the relationship between the PLL IC phase noise floor and the effective timing jitter present at the phase frequency detector output.

The Empirical Model

Consider a standard PLL frequency synthesizer as shown in Figure 1

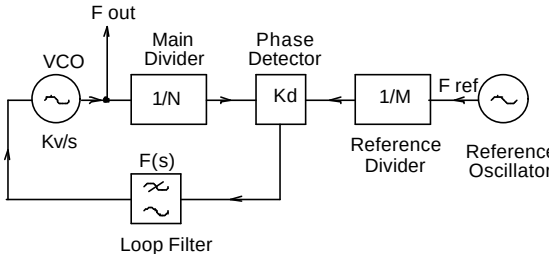

Figure 1 - Phase Locked Loop Synthesizer

It is known that within the PLL loop bandwidth the phase noise is typically dominated by noise added by the frequency dividers and phase detector. For frequencies well below the loop bandwidth the phase noise plot typically flattens out resulting in the *in-band phase noise floor*. A typical phase noise spectrum at the output of a PLL synthesizer is shown in Figure 2.

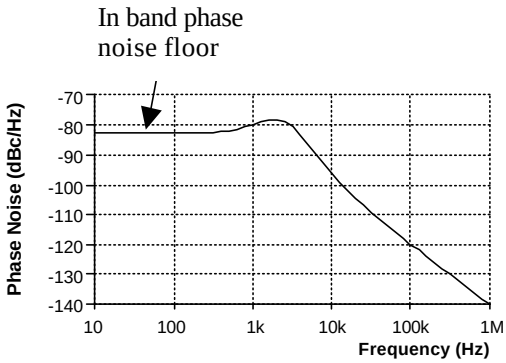

Figure 2 - Typical PLL Output Phase Noise

The in-band phase noise floor indicated in Figure 2 is approximately $L_{floor} \approx -82\text{dBc/Hz}$.

Banerjee [1] discovered that the noise contribution from the digital components in the PLL IC can be summarised into a single parameter, the 1Hz Normalized Phase Noise Floor, which can be determined from a particular measurement of L_{floor} by:

$$L_{1Hz} = L_{floor} - 20\log_{10}(N) - 10\log_{10}(F_c) \qquad \ldots (1)$$

where N is the division ratio in the loop and F_c is the phase comparison frequency. In any other application, the in-band phase noise floor from the PLL IC can be then determined by:

$$L_{floor} = L_{1Hz} + 20\log_{10}(N) + 10\log_{10}(F_c) \qquad \ldots (2)$$

This model was applied to a wide range of National PLL IC's in various applications giving usefully accurate predictions [1].

By substituting $N = \frac{F_o}{F_c}$ into (2) gives

$$L_{floor} = L_{1Hz} + 20\log_{10}(F_o) - 10\log_{10}(F_c) \quad \ldots (3)$$

which demonstrates that for a given PLL IC and desired output frequency, the phase noise floor may be decreased by 3dB by doubling the phase comparison frequency.

A slightly different rearrangement shows dependence of phase noise on N for fixed F_o.

$$L_{floor} = L_{1Hz} + 10\log_{10}(F_o) + 10\log_{10}(N) \quad \ldots (4)$$

Explaining the Empirical Model

Seeking insight into the problem, and indeed understanding of the validity of the empirical model (2), we look for physical processes that explain the relationship. As the equation is far from intuitive, we include two heuristic explanations before developing a more rigorous physical model based on the timing jitter at the phase detector. The first explanation is based on [1].

Explanation 1

Engineers understand that any noise on the reference frequency is multiplied by a factor N to the VCO output. Thus the output phase noise must have the $20\log_{10}(N)$ term shown in (2). Clearly if N were doubled in the PLL, keeping all other parameters constant, then the in-band phase noise would increase by 6dB.

We need to explain how, if we double the comparison frequency whilst keeping N constant, the output phase noise increases by 3dB. In this case, imagine that there is a fixed noise contribution on each phase detector current pulse. So doubling the comparison frequency will result in twice as many noise pulses to the loop filter, which leads to 3dB more noise. (It has to be assumed that the noise pulses are uncorrelated to make this conclusion.) This leads to the $10\log_{10}(F_c)$ term in (2).

Explanation 2

If the VCO is oscillating at a frequency $F_o = NF_c$ then the PLL IC is receiving F_o transitions per second. The effect of using a digital divider to divide by N is to estimate the VCO phase (for phase locking purposes) by considering only one transition out of each N. As a signal estimation problem, if we double N we throw away half of the information we were using and we would expect the S/N ratio of our phase estimate to degrade by 3dB, and so the phase noise to increase by 3dB. (Again we are assuming that the noise contributions at each transition are equal and uncorrelated.) So for fixed output frequency, we expect the phase noise to vary according to $10\log_{10}(N)$. This directly explains the relationship as presented in (4).

Now given that the phase noise floor varies according to $20\log_{10}(N)$ when F_c is fixed, as explained previously, so doubling N causes the $20\log_{10}(N)$ term to add 6dB, so the halving that occurs in F_c must cancel 3dB of this, so there must be a $10\log_{10}(F_c)$ term as well, leading to (2).

A Physical Model

Consider a model of a PLL IC as shown in Figure 3.

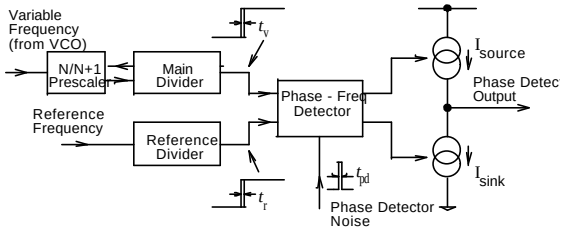

Figure 3 - PLL IC Phase Noise Model

It is apparent that at the output of the main divider there is timing jitter (denoted t_v seconds rms) from several possible sources:

- jitter produced at the input stage where the VCO waveform is quantised – both due to additive noise on the wanted signal and also to noise affecting bias and hence the slicing level
- jitter added by the dividers

At the output of the reference divider there is timing jitter (denoted t_r seconds rms) from similar sources in the reference signal path.

Depending on the state of the phase-frequency detector, either the edge from the main divider starts the current pulse output and the edge from the reference divider ends it, or vice versa. Thus the two timing jitters from the dividers cause a cumulative jitter in the width of the pulse from the charge pump, the rms variation of the jitter is given by

$$t_{dividers} = \sqrt{t_v^2 + t_r^2}$$

(assuming t_v and t_r are uncorrelated).

It is likely that with the use of synchronous dividers, that t_v and t_r are relatively unaffected by division ratios, provided that interactions between the two dividers are minimised and the divider architecture remains constant.

The phase-frequency detector (PFD) and charge pump will add noise of its own. The digital logic in the PFD will add further timing jitter as will the charge pump. In addition, many charge pump PFD circuits enable both charge pumps briefly to eliminate the phase detector dead spot. This results in some feedthrough of the charge pump current noise, (proportional to the activation time). To analyse this noise we propose to treat it as an additional timing jitter. It is likely that this is an accurate model for the case where the phase error is small (very short pulses from the phase detector), that is in the locked state. Thus the total noise from the PFD is included as the timing jitter t_{pd} in Figure 3.

So it is proposed that the noise from the PLL IC is modelled as timing jitter on the output pulse from the charge pump phase detector, total rms timing jitter given by

$$s = \sqrt{t_v^2 + t_r^2 + t_{pd}^2} \qquad \ldots (5)$$

Fractional-N Chips

The model can be extended to fractional-N chips which have in-built fractional compensation with a composite charge pump output. In this case, if we include t_{fc} as the timing jitter present at the PFD output from the fractional compensation, then the total timing jitter is given by

$$s = \sqrt{t_v^2 + t_r^2 + t_{pd}^2 + t_{fc}^2} \qquad \ldots (6)$$

Of course, the noise analysis of this is only accurate if the timing jitter is uncorrelated from sample to sample, that is the fractional compensation circuitry is successfully removing the fractional spurs and leaving only white noise.

Analysis of Timing Jitter

We will now analyse the effect on this timing jitter on PLL noise performance. The model will be applied to the charge pump phase frequency detector, but it is equally applicable to other implementations of the PFD.

The ideal phase-frequency detector with current pump output produces a pulse of current each phase comparison cycle, (essentially each reference edge) the duration of the pulse is proportional to the phase error. We assume that the kth comparison cycle occurs at time kT_c. Thus for phase error $f_e(kT_c)$ the ideal duration t_k of the current pulse is given by

$$t_k = \frac{f_e(kT_c)}{2p} T_c \qquad \ldots (7)$$

where $T_c = \frac{1}{F_c}$ with F_c the phase comparison frequency.

We now include a timing jitter, so that at time kT_c the current pulse has the ideal duration plus the timing jitter

$$t_k = \frac{f_e(kT_c)}{2p} T_c + t_k \qquad \ldots (8)$$

where the timing jitter is represented by t_k, a random variable with zero mean and variance $s^2 = \overline{t_k^2}$. Thus sometimes the pulses are too long, sometimes too short, the rms variation of the pulse width is s.

Consider the PLL shown in Figure 4

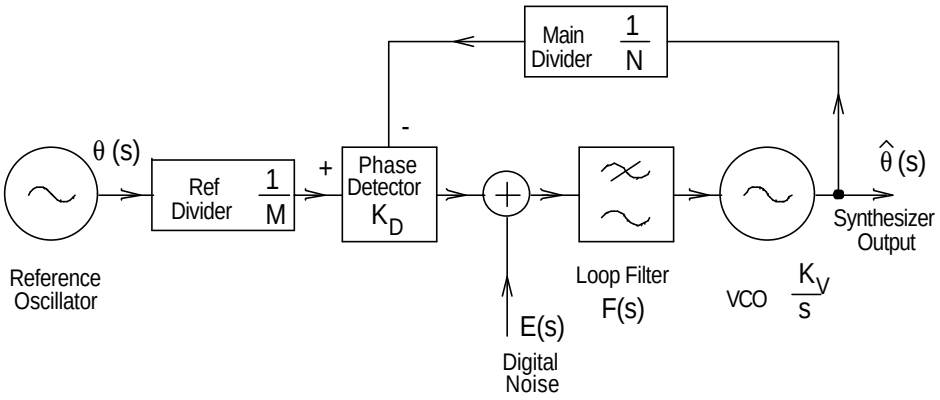

Figure 4 - PLL Block Diagram

We have removed all noise from the dividers and phase detector, and included the effect of the timing jitter as the "Digital Noise *E(s)*" added at the output of the phase detector in Figure 4. We denote the frequency domain representation of the noise by *E(s)* and the time domain waveform by *e(t)*. Now *e(t)* consists of random pulses of current, the length of the *k*th pulse is $|t_k|$. If t_k is positive then the pulse has length t_k and the current the same sign as the wanted pulse and, if t_k is negative then the pulse has length $|t_k|$ and the current the opposite sign to the wanted pulse. Thus the waveform of the digital noise *e(t)* is as shown in Figure 5

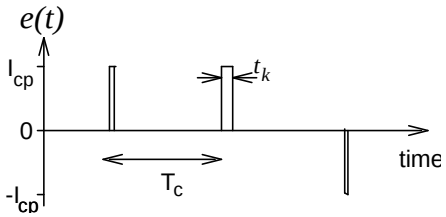

Figure 5 - Digital Noise Waveform

Returning to Figure 4, the output phase of the synthesizer is given by

$$\hat{q}(s) = q(s)\frac{N}{M}\frac{G(s)}{1+G(s)} + E(s)\frac{N}{K_D}\frac{G(s)}{1+G(s)} \qquad \ldots (9)$$

Within the loop bandwidth, where $|G(j2pf)| >> 1$, the contribution to the output phase noise from the digital noise is given by

$$\hat{q}(s)_{\text{digital noise}} = E(s)\frac{N}{K_D} \qquad \ldots (10)$$

So the in-band phase noise floor can be determined directly from the spectrum *E(s)* of *e(t)*.

The spectrum of *e(t)* is derived in Appendix A, giving the result that the in-band phase noise floor is

$$L_{floor} = 20\log_{10}(2ps) + 20\log_{10}(N) + 10\log_{10}(F_c) \qquad \ldots (11)$$

This is the same as equation (2) with

$$L_{1Hz} = 20\log_{10}(2ps) \qquad \ldots (12)$$

Thus, the empirical equation (2) is entirely consistent with there being a fixed amount of timing jitter present on the phase detector output, independent of the division ratio N and the phase comparison frequency F_c.

Numerical Results

Typical values for the 1Hz normalized phase noise floor published in [1] and other areas are in the range -200dBc/Hz to -220dBc/Hz. Table 1 shows the corresponding values of timing jitter.

L_{1Hz} dBc/Hz	RMS Jitter ps
-200	15.9
-210	5.0
-220	1.6

Thus, to produce a PLL IC with state of the art L_{1Hz} of around -215dBc/Hz requires the effective rms timing jitter of the phase detector output pulses to be no more than 2.8ps.

Fractional-N synthesiser chips may be treated here as simply providing a non-integral value of N. The modern chips provide internal fractional spurious compensation. With no fractional spurious compensation, the rms timing jitter at the phase detector would be both large (lots of phase modulation) and have correlation between samples (giving discrete spurs). For the modern chips that contain internal spurious compensation, the net effect is that in fractional mode all that is apparent from outside the chip is a random timing jitter at the phase detector. As long as there are no large discrete spurious components, then (11) should still be applicable.

It is also easy to derive from these results the slicing accuracy required on the VCO and reference frequency inputs to the PLL IC. Sinusoidal reference waveforms of the typical 1V p-p become problematic at frequencies of the order of 10MHz and below due to the difficulties of digital conversion with low picosecond jitter.

Factors influencing L_{1Hz}

The model of the phase noise contribution by the PLL chip given by (11) is only of great use if we are able to use measurements of L_{1Hz} made in one PLL to predict L_{1Hz} in other PLL's.

It is known that the phase noise floor often varies with charge pump current [1], typically improving at higher currents. It is difficult to speculate on the exact details of this without knowing the implementation details of specific charge pumps, however some manufacturer's outline schematics indicate that the high-current charge pump is achieved by the parallel operation of multiple charge pumps. In this case it would be expected that the charge pump noise would drop by 3dB each time the number of charge pumps was doubled (assuming that the noise from each was uncorrelated). This should apply both to the timing jitter noise and also to any current noise feedthrough due to the minimum

pulse width. Any correlation between the noise from individual pumps would lead to a lesser benefit.

As the fundamental cause of L_{1Hz} is timing jitter, other factors that affect the timing jitter may affect L_{1Hz}. A significant source of variability here for some modern chips may be the operating voltage, as many devices can operate over a considerable range of power supply voltages.

Also, in any application, it is essential to ensure that the slicing jitter added at the VCO and reference inputs does not dominate L_{1Hz}, degrading the performance of the PLL IC.

Conclusions

It has been shown that the empirical relationship published relating the phase noise contributed by the PLL dividers and phase detector are consistent with a consistent random timing jitter present on the pulses at the output of the phase detector. The relationship between the effective timing jitter and the phase noise has been derived.

REFERENCES:

1. Banerjee, Dean "PLL Performance, Simulation and Design" National Semiconductor 1998 www.national.com
2. "SimPLL" – PLL design and simulation software, www.radiolab.com.au

Appendix A – Derivation of Equation 11

The noise waveform resulting from the timing jitter is shown in Figure 5.

To compute the power spectral density of this waveform, it is possible to proceed conventionally by computing the autocorrelation function and then taking the Fourier transform, however it is easier to proceed directly:

The two sided power spectral density *S(f)* of a noise process *x(t)* is defined as

$$S(f) = \lim_{T\to\infty} \frac{\overline{|X_T(f)|^2}}{T} \text{ where } X_T(f) = \int_{-\infty}^{\infty} x(t)e^{-j2pft}dt$$

so

$$E(f) = \lim_{T\to\infty} \frac{1}{T}\overline{\left|\int_{-T/2}^{T/2} e(t)e^{-j2pft}dt\right|^2}$$
$$= \lim_{T\to\infty} \frac{1}{T}\overline{\left|\sum_{\text{N terms}} I_{cp}t_k e^{-j2pft}\right|^2}$$

..(A1)

where $N = TF_c$, the number of phase detector pulses in the integration time. As we are assuming that the jitter periods are uncorrelated, then

$$E(f) = \lim_{T\to\infty} \frac{TF_c I_{cp}^2 s^{\,2}}{T} \quad \text{as } < t_k^2 >= s^{\,2}$$
$$= I_{cp}^2 s^{\,2} F_c$$

..(A2)

The single-sided PSD is given by *E(f)*, so the rms phase deviation in a 1Hz bandwidth around *f* is

$$q_{\text{rms dev}} = \sqrt{2E(f)}\,\frac{N}{K_D}\frac{G(j2pf)}{1+G(j2pf)}$$

..(A3)

including a factor of 2 as *E(f)* is double-sided. The relationship between SSB phase noise sidebands and rms phase deviation is

$$L_f(f) = \frac{q_{\text{rms dev}}}{\sqrt{2}}$$

and so

$$L_f(f) = \sqrt{E(f)}\,\frac{N}{K_D}\frac{G(j2pf)}{1+G(j2pf)}$$

..(A4)

which, using $K_D = \frac{I_{cp}}{2p}$ gives an in-band ($|G(j2pf)| >> 1$) phase noise floor of

$$L_{floor} = 2ps\sqrt{F_c N}$$

..(A5)

or

$$L_{floor}(\text{dBc/Hz}) = 20\log_{10}(2ps) + 10\log_{10}(F_c) + 20\log_{10}(N)$$

which is equation (11).

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